# EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 0 | (customiz$4 development demonstration platform structured asic slice programmable processor high speed serdes fpga port driv$4 test signal integrity electrical characteristic (IP or intellectual) pin$4 link layer). clm. | USPAT | AND | ON | 2006/12/08 15:01 |
| S1 | 1141 | (716/16-17).CCLS. | US-PGPUB; USPAT | OR | OFF | 2006/12/08 11:53 |
| S2 | 1 | ("6347395").PN. | US-PGPUB; USPAT | OR | OFF | 2006/12/08 12:35 |
| S3 | 10 | "6347395".uref. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/08 12:26 |
| S4 | 38 | fpga and asic and (serdes (serializer near2 deserializer)) and port and slic$3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/08 12:40 |
| S5 | 5 | rapidslice | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/08 12:37 |
| S6 | 1 | asic same platform same serdes same slice | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/08 12:41 |
| S7 | 1 | ("20060193346").PN. | US-PGPUB; USPAT | OR | OFF | 2006/12/08 13:32 |
| S8 | 0 | structure$2 asci fpga serdes port test (ip or (intellectual near3 property)) high near2 speed layer $6slice | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | AND | ON | 2006/12/08 12:59 |
| S9 | 0 | structure$2 asci fpga serdes port (ip or (intellectual near3 property)) high near2 speed layer $6slice | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | AND | ON | 2006/12/08 13:00 |

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|---|---|---|---|---|---|---|
| S10 | 0 | structure$2 asci fpga serdes port $6slice | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | AND | ON | 2006/12/08 13:00 |
| S11 | 9 | structure$2 asic fpga serdes port (ip or (intellectual near3 property)) high near2 speed layer $6slice | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | AND | ON | 2006/12/08 13:03 |
| S12 | 1163 | (716/18).CCLS. | US-PGPUB; USPAT | OR | OFF | 2006/12/08 13:05 |
| S13 | 616254 | asic slice platform custom | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/08 13:05 |
| S14 | 51 | asic slice platform custom$6 serdes | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | AND | ON | 2006/12/08 13:06 |
| S15 | 51 | asic slice platform custom$6 serdes (fpga or ((field or programmable or gate) near4 array)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | AND | ON | 2006/12/08 13:08 |
| S16 | 103 | asic platform custom$6 serdes (fpga or ((field or programmable or gate) near4 array)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | AND | ON | 2006/12/08 13:08 |
| S17 | 52 | S16 not S15 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | AND | ON | 2006/12/08 13:20 |
| S18 | 1 | ("20050183042").PN. | US-PGPUB; USPAT | OR | OFF | 2006/12/08 13:20 |
| S19 | 1 | S18 and (prov$3 near3 concept) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/08 13:26 |
| S20 | 264 | (asic same (prototyp$4 or develop$5)) and (fpga same external) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/08 13:27 |

# EAST Search History

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|---|---|---|---|---|---|---|
| S21 | 34 | (asic same (prototyp$4 or develop$5)) and (fpga same external) and slice | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/08 13:31 |
| S22 | 1 | (asic same (prototyp$4 or develop$5)) and (fpga same external) and slice and (serdes or gigablze) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/12/08 13:28 |

**Web** Results **1** - **10** of about **494** for **structured asic platform fpga serdes port test IP layer**. (**0.38** seconds)

NEC Electronics Press Release: June 9, 2003
With the introduction of ISSP2 **structured ASIC** devices, NEC Electronics builds on ... third-party **IP** vendors to **port** their **IP** cores to the ISSP **platform**. ...
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Using ISSP technology in **structured ASIC** design
**FPGA**,**ASIC** and multichip sili-. con conversions, will do like- ... vited to **port** their **IP** cores to. the ISSP **platform**. After certi-. fication, **IP** cores such ...
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tous **structured ASIC** design. **platform**. Under the program, ... vited to **port** their **IP** cores to. the ISSP **platform**. After certi-. fication, **IP** cores such as ...
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SOCcentral: **Structured ASIC** Platforms with Integrated **SerDes** Cores ...
So integrating **SerDes** cores into **structured ASIC platform** is an excellent strategy. ... Universities involved in SoC, **ASIC** and **FPGA** design, EDA tools & **IP**. ...
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**Structured ASICs** & **Platform** FPGAs ... directory of Vendors, Organizations & Universities involved in SoC, **ASIC** and **FPGA** design, EDA tools & **IP**. ...
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Soft **IP** core. VHDL and Verilog RTL for **ASIC**, **Structured ASIC**, and **FPGA** ... **platform**. hard. w. a. r. e. **platform**. 8 **SerDes**. Xilinx Virtex-4 LX **FPGA** ...
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[PDF] DesignCon 2005 Customized Synthesis for 90 nm **Structured ASICs** ...
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The **structured ASIC platform** achieves this shorter development cycle by ... ISSP90 devices will incorporate a 10 Gbps single-**port SerDes** interface as well ...
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Many designers use the terms **platform** and **structured ASIC** interchangeably, ... a dozen

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Inventors: **Danny Vogel**, **Carl Shaw** Class: 716001000 (USPTO) ... [0005] Development of a **structured ASIC** often creates a need not only for a demonstration ...
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**Structured ASIC** architectures were designed to reduce and even eliminate some ... **Karl** Bois, Signal-Integrity Engineer, Hewlett-Packard. **Shaw** Moldauer ...
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